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09/854,038	05/11/2001	Richard J. Grupp	BUR920000214US1	8170

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/854,038	RICHARD J. GRUPP	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/5/2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,5,12-14,16,18-22,26 and 28-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,5,12-14,16,18-22,26,28-36,39-41 and 44-46* is/are rejected.

7)☒ Claim(s) *37-38, 42-43, 47-48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4, 6-11, 15, 17, 23-25 and 27 are cancelled. The amended claims 3, 5, 12-14, 16, 18-22, 26 & 28-33 and new claims 34-48 are presented for reconsideration as filed on 5th April 2005 by the applicant.
2. Claims 12-16, 3, 5, 34-36 from first claim tree, claims 18-21, 39-41 from second claim tree and claims 22, 26, 28-3, 44-46 from third claim tree are rejected.
3. No new references are applied. New art pertinent to this case has been cited in new PTO 892.
4. Claims 37-38, 42-43 and 47 & 48 are objected to.

Response to Applicant's Remarks

5. The arguments submitted by the applicant have been fully considered. The examiner's response is as follows.

35 USC § 101

6. The examiner thanks the applicant for amending the claims to address 35 U.S.C. §101 issues in claims 1-10, 11-16, 22-23, 25-33 and rescinds all related rejections.

35 USC § 103

7. Applicant argued:

> "... that claims 12, 20, and 22 are not unpatentable over Huang in view of Chandra '955, because Huang in view of Chandra '955 does not teach or suggest each and every feature of claims 12, 20, and 22. For example, Huang in view Chandra '955 does not teach or suggest the feature of: the first path including a second NMOS device, and a fourth NMOS device, and the second path including a first NMOS device and a third NMOS device.".

Examiner respectfully traverses the applicant argument and disagrees. Huang teaches two paths (Huang '593: Figure 1, Elements 11 & 13). Further Huang '593 teaches first path including an NOR gate (Huang '593: Fig 1, Elements 26) and buffer (Huang '593: Fig 1, Elements 16), each of which include at least one NMOS device each. It is well known in the art that conventional NOR gate design includes at least one NMOS device. Although the examiner had not referenced this as prior art, because conventional NOR gate including NMOS device is well known in the art, it was cited in reference "A symmetric CMOS NOR Gate for High Speed Applications" (Johnson 1988 hereafter) as Fig 1(a), attached to office action mailed previously. Further, the buffer disclosed in Huang contains at least one NMOS device (Huang '593: Fig. 2). Although Huang teaches buffer components comprising of transistors, the schematic in Fig 2 for the transistor is conventional symbol for the

NMOS device and is well known in the art. Hence each path consists of at least two NMOS devices, one each from NOR gate and buffer.

8. Applicant argued:

> "While Huang discloses that the buffer 16 comprises transistors T1 and T2, Huang does not disclose that the transistors T1 and T2 are NMOS transistors."

Although Huang discloses the transistors as buffer components, the schematic symbol for the transistor (Huang '593, Fig. 2) is conventional symbol for the NMOS device and is well known in the art.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to modify the teachings suggested by Huang, as suggested by the conventional knowledge of art and Fig 2 from Huang to implement the design with NMOS. The motivation would have been Fig 2-suggestion itself about using NMOS device and the fact that Huang is moot on to the fact that the transistors could be either NMOS or PMOS (CMOS based design).

9. Applicant argued:

> "Applicants disagrees with the Examiner's contention that Huang inherently discloses an NMOS device in the NOR gates 24 and 26 of Fig. 1 of Huang... The two switches A and B may comprise transistors but may be alternatively be switches not comprising transistors. Moreover, even if the switches A and B comprise transistors, the transistors do not have to be NMOS transistors."

Examiner agrees with applicant that Huang '593 does not disclose NOR gate comprising transistors, but it would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to use transistor in Huang's NOR gate design. The motivation would have been that Huang's buffer design, the other component of the model, comprises transistors (Huang'593: Col.Col.3, Lines 46-49). Further the since Huang '593 is moot on the design of the NOR gate it would be obvious to use the conventional design of NOR gate which is well known in the art the time the invention was made. Johnson 1998 (as disclosed in paragraph numbered 7 above) teaches the conventional NOR gate design using transistors with CMOS (NMOS & PMOS both).

10. Applicant argued:

> "Moreover, inherency cannot be used to reject a claim under 35 U.S.C. §103(a)..."

Examiner agrees that inherency cannot be used to reject claim under 35 U.S.C. §103(a). Examiner apologizes for the editing error in the language of the previous office action and thanks the applicant for pointing out that the correct term of use should have been "obvious". As stated above in paragraph 5, the NOR gate design would have been obvious to one of ordinary skill in the art, in view of Huang's suggestion.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 12, 3, 5, 16, 18, 20, 22, 26, 28-29, 33-35, 39-40, 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 5,202,593 issued to Huang et al (Huang '593 hereafter) in view of US Patent 6,496,955 issued to Chandra '955 et al (Chandra '955 '955 hereafter).

Regarding Claim 12

Huang '593 discloses in Fig.1, a first path (element 13) between first port (element 12) and second port (element 14). Further, Huang '593 discloses in Fig.1, a second path (element 11) between second port (element 14) and first port (element 12).

Huang '593 also discloses a buffer, a three-input NOR-gate and a single-shot device (Huang '593: Col. 2-Line54-56). NOR gate and a single-shot device act as control mechanism (Huang '593: Col. 1-Line 20-22). The control mechanism senses the change between the ports (Huang '593: Fig.1-Element 12 & 14) with corresponding to signals S1 and S2 and drives the second port with the same input signal as the first port (Huang '593: Col. 2-Line 28-37). The control mechanism also enable the appropriate path by disabling the second path until the driving signal is

asserted on the first port (Huang '593: Col. 2-Line 38-47), hence only one path is driving the ports at any given time. The same reasoning works when the signal is asserted on the second port and it drives the first port. Further, Claim 12 is rejected as Huang '593 teaches a buffer (Huang '593: Fig. 2), which is a pass device comprising of NMOS devices (conventional symbol).

Huang '593 does not disclose that circuit is a *model for representing a bidirectional wire* [bus] *input/output (I/0) during computer simulation.*

Chandra '955 teaches us that a module[1] can be represented in high-level HDLs such as Verilog hardware description language (HDL) or VHDL written in RTL or transistor level using primitives provided by HDL (Chandra '955: Col. 4-Line 7-20). Verilog or VHDL module is a model of actual circuit that can be executed on a computer and Chandra '955 teaches us how create such a module (Chandra '955: Col. 4-Line 21-44, Line 60-67) by example.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to modify the teachings suggested by Huang '593 and implement them in Verilog or VHDL as disclosed by Chandra '955. Chandra '955's teachings would allow users of Huang '593's circuit to perform circuit analysis on a bi-directional I/O wire in an expeditious manner through simulation. Issues like timing constraints can be addressed and captured at simulation time before fabrication of the actual circuit containing bidirectional I/O wires is done. Further motivation comes from Chandra '955 as he teaches the need to perform functionality

checks and other simulations of the models in view of growing complexity of digital systems (See: Chandra '955, background).

Regarding Claim 3

Claim 3 is rejected as Chandra '955 teaches that HDLs like Verilog or VHDL can be used to implement the model (Chandra '955: Col. 4-Line 7-20).

Regarding Claim 5

Huang '593 discloses a quiescent state when no external buses (net) are driving the ports. The ports remain in high logic level (Huang '593: Col. 1-Line 36-40). When one of the external nets drives input net [port] (Huang '593: Fig.1 element 12) low, the first unidirectional path (Huang '593: Fig.1 element 13) pulls the other net [port] low (Huang '593 Fig.1 element 14; Col. 1-Line 40-42). A control signal is also issued to the disable the other unidirectional path (Huang '593: Fig.1 element 11) (Huang '593: Col. 1-Line 50-65). The 3-input-NOR (Huang '593: Fig.1 element 26) in the first path (Huang '593: Fig.1 element 13) feeds back on 3-input-NOR (Huang '593: Fig.1 element 24) in the second path (Huang '593: Fig.1 element 11) through input AU (& AD). This feedback input from first path enables (or disables) the second path. This input goes into an NMOS device, which is comprised in the 3-input-NOR gate (as mentioned in the conventional 3-input-NOR design in the preceding claim). Hence, Huang '593 replicates the mechanism mentioned in the claim 5.

Regarding Claim 16

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[1] A module can represent pieces of a hardware system ranging from simple logic gates to complete systems, e.g. a computer. In our case this module is a circuit.

Huang '593 discloses that the control mechanism disables the second path until the driving signal is asserted on the first port [and path] (Huang '593: Col. 1-Line 50-65), hence only one path is driving the ports at any given time. Observing the Fig.1, this is true vice versa also.

Regarding Claim 18

Huang '593 discloses that the control mechanism disables the second path until the driving signal is asserted on the first port [and path] (Huang '593: Col. 1-Line 50-65), hence only one path is driving the ports at any given time. Observing the Fig.1, this is true vice versa also.

Regarding Claim 20

Claim 20 is rejected for the same limitations in part as claim 12, with Huang '593 in view of Chandra '955. Further, Huang '593 discloses details of a buffer (Huang '593: Fig. 2) and 3-input-NOR gate (Huang '593: Fig.1 elements 24 & 26). The buffer comprises of two NMOS (Huang '593: Fig 2) as symbolic representation and only one of them in the path at any given time. Huang '593 does not teach that 3-input-NOR gate comprises NMOS gate.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to use transistor in Huang '593's NOR gate design based on the conventional knowledge and advantages of CMOS design well known in the art. The motivation would have been that Huang '593's buffer design, the other component of the model, comprises transistors (Huang '593: Col.Col.3, Lines 46-49). Further, Huang '593 is moot on the design of the NOR gate it would be obvious

to use the conventional design of NOR gate which is well known in the art the time the invention was made. The convention design as described by Johnson 1998 in paragraph 7 above uses transistors, both PMOS and NMOS to implement a NOR gate. Hence as claimed the each path would have at least 2 NMOS devices.

Regarding Claim 22

Claim 22 part A recites same claim limitations as claim 12. 22-A is rejected for afore mentioned reasons for claim 12. Additionally, it includes a "recoding media" in part B of the claim.

Disclosure by Huang '593 is mentioned before in claim 12. Huang '593 does not teach a about a recording media bearing the hardware description language (HDL) model. Further, Huang '593 does not teach that 3-input-NOR gate comprises NMOS gate.

Chandra '955 teaches that a model could be captured in a HDL [RTL description] and stored on a storage device, which communicates with a computer (Chandra '955: Col. 5-Line 66-67, Col. 6-Line 1-3).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made that teaching of Chandra '955 can be applied to Huang '593 to store the model on a storage device [recordable media]. The motivation would be the ability to retrieve from storage device the model to simulate & test the behavior of bidirectional I/O wire. Further the motivation to use the NMOS devices in the NOR gate would have been the same as mentioned in the claim 20 rejection above.

Regarding Claim 26

Claim 26 is rejected as Chandra '955 teaches that HDL's like Verilog or VHDL can be used to implement the model (Chandra '955: Col. 4-Line 7-20).

Regarding Claim 28

Claim 28 is rejected for the same reasons as claim 5 mentioned above.

Regarding Claim 29

Claim 28 is rejected, as Chandra '955 in view of Huang '593 teaches that circuits can be modeled using Verilog or VHDL. Hence the NMOS device could be modeled using Verilog NMOS primitives when Verilog is used as HDL.

Regarding Claim 33

Huang '593 teaches that the control mechanism disables the second path until the driving signal is asserted on the first port [and path] (Huang '593: Col. 1-Line 50-65), hence only one path is driving the ports at any given time. Observing the Fig.1, this is true vice versa also.

Regarding Claim 34

Huang '593 teaches a first path (Huang '593: Fig.1, Element 11) and a second path (Huang '593: Fig.1, Element 13) parallel to each other. Huang '593 teaches details of a buffer (Huang '593: Fig. 2) and 3-input-NOR gate (Huang '593: Fig.1 elements 24 & 26) in series as can be seen from Fig.1. The buffer comprises of two NMOS (Huang '593: Fig 2) as symbolic representation and only one of them in the path at any given time. Huang '593 does not teach that 3-input-NOR gate comprises NMOS gate.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to use transistor in Huang '593's NOR gate design based on the conventional knowledge and advantages of CMOS design well known in the art. The motivation would have been that Huang '593's buffer design, the other component of the model, comprises transistors (Huang '593: Col.Col.3, Lines 46-49) and it would be obvious to make other components from transistors as well. Further the since Huang '593 is moot on the design of the NOR gate it would be obvious to use conventional design of NOR gate which is well known in the art the time the invention was made. The convention design as described by Johnson 1998 in paragraph 7 above (Page 3) uses transistors, both PMOS and NMOS to implement a NOR gate. Hence Huang '593 teaches each path would have at least 2 NMOS devices in series because the NOR gate and buffer are in series.

Regarding Claim 35

Huang '593 teaches that control mechanism, without any external signal (Huang '593: Col.4 Lines 4-10), detects the change on both the first and second port to determine which port needs to actively drive the signal. Huang '593 does teach that the HDL register values are used to detect changes on the two ports.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to use HDL register in Huang '593's design to detect port value changes. Huang '593 does teach that in bidirectional repeater the port status is preset to ports being driven high when no one port driving the bus and

then detecting change based on this preset from either ports, which is equivalent to having a HDL register to detect state change (Huang '593: Col.1, Lines 33-49). The motivation would have been that function of both HDL register and Huang '593's preset on the bus are the same, i.e. to detect the change in the port statuses.

Regarding Claim 39

Claim 39 is directed towards the same limitations as claim 34 and is rejected for the same reasons as claim 34.

Regarding Claim 40

Claim 40 is directed towards the same limitations as claim 35 and is rejected for the same reasons as claim 34.

Regarding Claim 44

Claim 44 is directed towards the same limitations as claim 34 and is rejected for the same reasons as claim 34.

Regarding Claim 45

Claim 45 is directed towards the same limitations as claim 35 and is rejected for the same reasons as claim 35.

12. Claim 13, 14, 19, 21, 30-32, 36, 41, 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 5,202,593 issued to Huang '593 in view of US Patent 6,496,955 issued to Chandra '955, further in view of in view of US Patent 5,396,435 issued to Ginetti (Ginetti '435 hereafter).

Regarding Claim 13

Huang '593 in view of Chandra '955 disclose a bidirectional I/O modeled in Verilog using NMOS gates as discussed above in claim 12 rejection.

Huang '593 and Chandra '955 do not teach annotated timing values to include the input port delays from the NMOS.

Ginetti '435 discloses that timing path delay values at an input port of a primitive cell is represented by a capacitance (Ginetti '435: Col. 2-Line 35-55).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to take the teachings of Ginetti '435 and apply them to Huang '593 & Chandra '955's teachings. They would teach that in a Verilog model created by Huang '593 & Chandra '955, delays in the primitive cells, like NMOS cells, could include input port delays. Hence timing values annotated in the model can include input port delays. The third NMOS would map to the NMOS in the buffer (Fig.1 element 18 instance of Fig2, element T1 & T2) and the forth NMOS would map to the NMOS in the buffers as well (Fig.1 element 16 instance of Fig2, element T1 & T2). The motivation to annotate the values in the timing of the any NMOS cell would be to get more realistic timing delay across the bidirectional wire I/O model/method and to meet timing constraints (Ginetti '435: Col.2 Lines 6-12).

Regarding Claim 14

Claim 14 is rejected as Ginetti '435 teaches delays are calculated between the first port and second port and vice versa. Ginetti '435 also discloses that the timing delays further include load dependent delays and port capacitances (Ginetti '435: Col. 2-Line 40-42). Ginetti '435 goes on to give all the delay components to annotate the timing information (Ginetti '435: Col. 2-Line 43-55) between the input and the output ports of a primitive cell (e.g. primitive NMOS device).

Regarding Claim 19

An analysis of Fig.1 (Huang '593) reveals that Huang '593 & Chandra '955 teaches the claimed controlled circuit wherein it can be seen from Fig. 1 that unidirectional paths (Huang '593: Fig.1 elements 11 & 13) comprise of control circuit (Huang '593: Fig.1, element 20, 26, 24 & 22) and output buffers (16 & 18), which can be modeled into Verilog or VHDL primitives & gates.

Huang '593 & Chandra '955 do not disclose annotating the timing on the two unidirectional paths that he discloses.

Ginetti '435 discloses that timing path between input and output of each primitive cell is approximated by gate propagation delay (Ginetti '435: Col. 2-Line 35-43).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to modify the teachings suggested by Ginetti '435 and apply them to Huang '593 & Chandra '955, by breaking up each path into individual subcomponents and primitive cells and then adding up the gate propagation delay information to annotate the timing values across the first path and

second path. Hence, Ginetti '435's teachings would allow user of the Huang '593 & Chandra '955's system to more accurately calculate the delays between the two unidirectional paths. Further, Ginetti '435 teaches that any circuit can be modeled into a Verilog or VHDL (Ginetti '435: Col. 1-Line 59-64).

Regarding Claim 21

Claim 21 is directed towards the same limitations as claim 13 and is rejected for the same reasons as claim 13.

Regarding Claim 30

Claim 30 is directed towards the same limitations as claim 13 and is rejected for the same reasons as claim 13.

Regarding Claim 31

Claim 31 is directed towards the same limitations as claim 19 and is rejected for the same reasons as claim 19.

Regarding Claim 32

Claim 32 is directed towards the same limitations as claim 14 and is rejected for the same reasons as claim 14.

Regarding Claim 36

Teaching of Huang '593 are disclosed in claim 35 rejections above. Huang does not explicitly teach holding the gates of third and forth NMOS devices high. Holding the gates high on third and forth NMOS devices is equivalent to having a wire/short between the drain & source, rendering them futile as far as signal control. From the

delay-modeling perspective, Huang '593 also uses transistor devices and delay can be modeled in his transistors using the same process as provided in specification.

Ginetti '435 discloses that timing path between input and output of each primitive cell (transistor/NMOS/PMOS) is approximated by gate propagation delay (Ginetti '435 Ginetti '435: Col. 2-Line 35-43) that can be modeled in HDL (Ginetti '435: Col. 1-Line 59-64).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to modify the teachings suggested by Ginetti '435 and apply them to Huang '593 & Chandra '955, by breaking up each path into individual subcomponents and primitive cells and then adding up the gate propagation delay information. The motivation would have been to calculate delays more realistically in a given circuit (Ginetti '435: Col. 2 Lines 30-37). Hence Ginetti'435, Huang'593 & Chandra'955 teach the function of third and forth NMOS devices.

Regarding Claim 41

Claim 41 is directed towards the same limitations as claim 36 and is rejected for the same reasons as claim 36.

Regarding Claim 46

Claim 46 is directed towards the same limitations as claim 36 and is rejected for the same reasons as claim 36.

End of Claim Rejection under 35 USC § 103.

Allowable Subject Matter

13. Claim 37-38, 42-43 and 47 & 48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is an examiner's statement of reasons for allowance: Although the concept of modeling the bidirectional wire with HDL is well known in the art, a prior art search of this particular implementation has failed to uncover the claimed exact circuit structure for the bidirectional wire model for the purpose of simulation.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

End of Allowable Subject Matter.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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May 3, 2005

JEAN R. HOMERE
PRIMARY EXAMINER